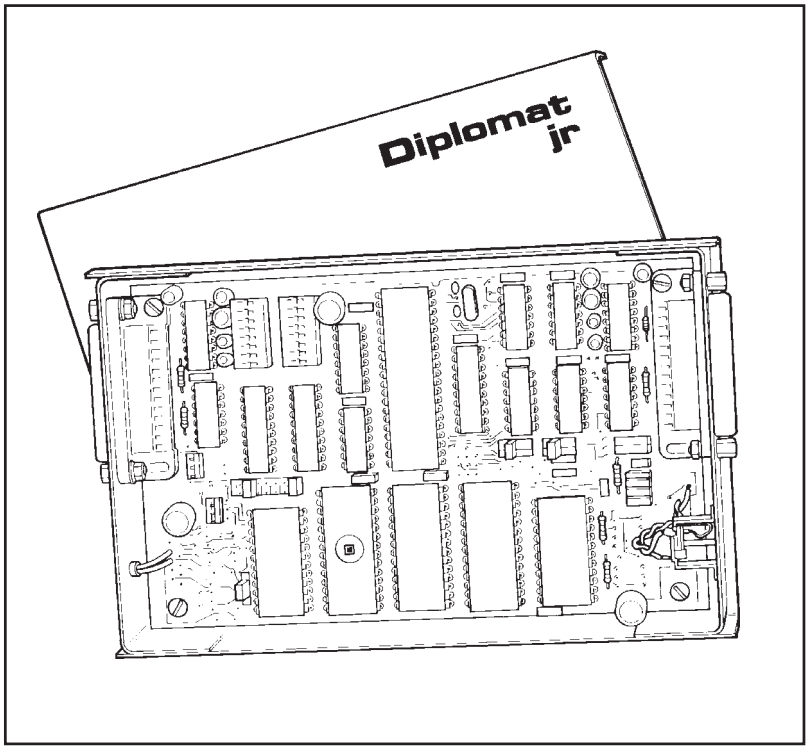
Lucidata Diplomat jr
User Guide
Model SA1TH (Special)



Lucidata House
Selwyn Close
Great Shelford
CAMBRIDGE CB2 5HA

tel: +44 (0) 1223 846100
fax: +44 (0) 1223 846100
email: docs@lucidata.com

Publication Details

All possible care has been taken in the preparation of this publication, but Lucidata accepts no liability for any inaccuracies that may be found.

Lucidata reserves the right to make changes without notice to both this publication and to the product which it describes.

If you find any errors in this publication or would like to make suggestions for improvement, please write to the Company at the address below.

Lucidata Data Communications Consultants
Lucidata House
Selwyn Close
Great Shelford
CAMBRIDGE CB2 5HA
England

tel: +44(0)1223 846100
fax:+44(0)1223 846100
email:docs@lucidata.com

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All Lucidata products are designed, developed and tested under the control of its ISO9000 compliant Quality Management System. The high quality of our products is thus assured. Should any issues on the quality of our products arise please address them to the Quality Manager at the address given on page 2. This User Guide contains all the necessary information for the proper installation and configuration of the product to ensure the highest level of performance.

Warranty

Lucidata warrants that the products described in this User Guide are free from defects in manufacture and that they meet the specifications and functionality described in this User Guide. Lucidata will replace parts and repair defects in manufacture, on a return to factory basis, for a period of 12 months from the date of our original invoice provided that the product has only been used in the manner and for the purpose described in this User Guide. Lucidata does not warrant that the products described in this User Guide are suitable for any specific application and the purchaser must satisfy him/herself of the suitability of the product for the intended application as best known to him/herself. Lucidata does not accept any contingent liability for any damages whatsoever including direct, indirect, incidental, consequential, loss of business profits or special damages arising from the use of its equipment. Lucidata assumes that if its equipment is used in a business critical or any other essential application, then the system design should incorporate sufficient resilience to ensure that a single failure would not have disproportionate consequences.

Service and Support

Should a Lucidata product appear to fail you should, in the first instance, contact your supplier who will be able to advise you and possibly solve your problem. If you contact Lucidata you should have the product description, serial number, date and place of purchase at hand so that we can efficiently identify your unit. If after assistance from our technical staff it appears that there is a failure you will be given a Returns Number to mark the package returned to the Lucidata factory. Units will be repaired free of charge if they are within warranty. Outside the warranty period repairs will be charged at Lucidata's normal rates. You will be given an estimate of the repair cost prior to work commencement.

Lucidata reserves the right to charge for any investigation it undertakes if the apparent fault is due to improper operation of the unit, or if the unit has been damaged by usage outside the scope of this User Guide.

Telephone support will be provided to all registered users of *Diplomat* units, during normal UK working hours. It is helpful if configuration difficulties or special situations are written down in words or a diagram and either faxed or emailed before telephoning. Support provided in person will be chargeable at a time-and-materials rate. Please contact Lucidata for details.

Product Upgrades

From time to time Lucidata may offer upgrades of firmware to existing registered users of *Diplomat* units.

Full instructions for implementing any such upgrade will accompany the upgrade pack.

Safety

This product is for indoor use only and should NOT be operated with the lid removed. It contains devices which are static sensitive. Great care should be taken when adjusting switches and links to avoid touching any connections. Whenever possible, anti-static precautions should be taken, such as the use of an earthed wrist-strap and anti-static mat.

PRODUCT DETAILS

Product name ***Diplomat*™ jr**

Model SA1TH

Serial Number 0825+

Configuration Code 000

Firmware Reference SA1TH Rev. 1.00

Issue Date 28/08/06

Special features/notes

Note: Special version built to customer specifications - see Appendix A

About the Diplomat jr

Lucidata *Diplomat* protocol convertors enable interconnection of computer equipment from different manufacturers.

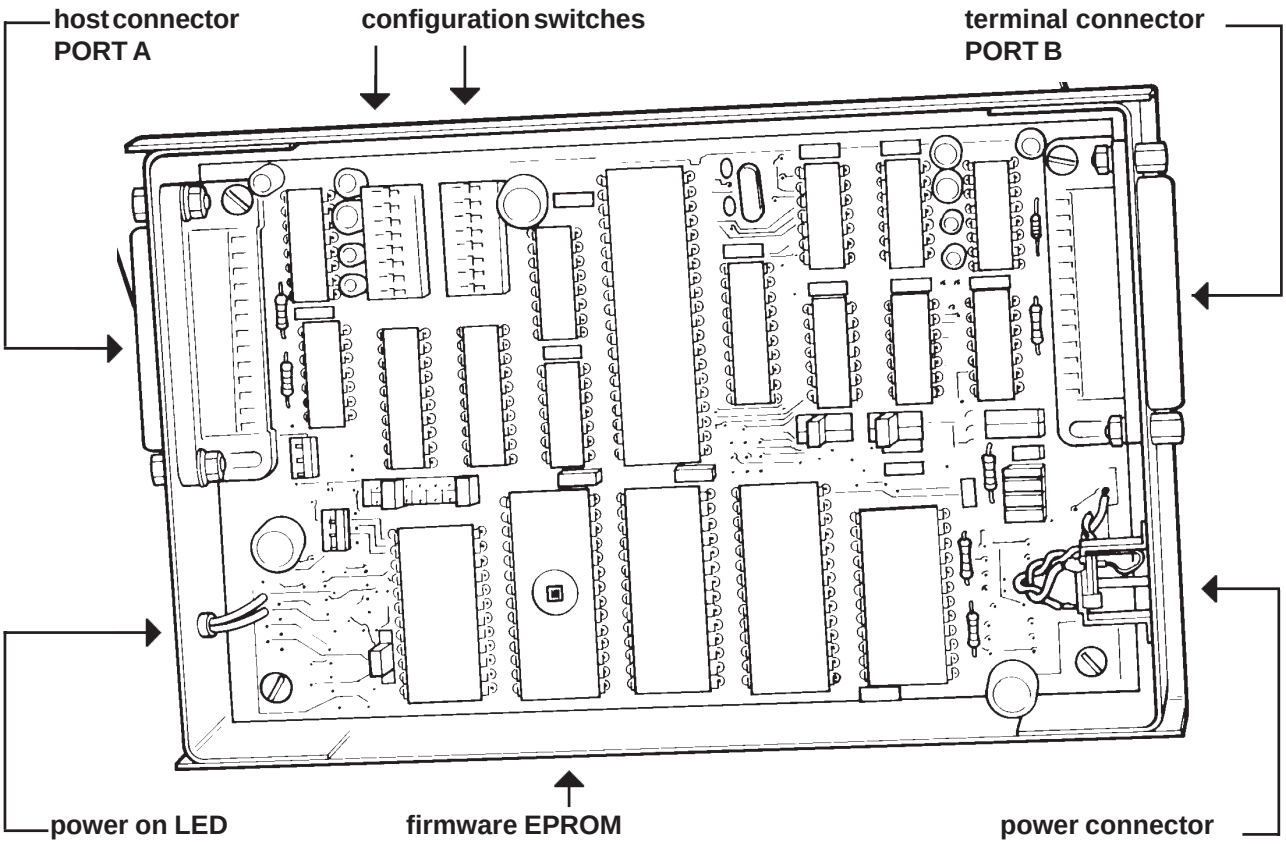
Equipment A **Diplomat jr** **Equipment B**

The *Diplomat jr* models are all designed to connect two pieces of equipment using serial RS232 data streams operating at different data rates and character formats.

The *Diplomat jr* is housed in a black aluminium case and is powered from an external mains adaptor.

The unit contains advanced digital electronic circuitry which performs the required function under the control of the **firmware**, contained in a single integrated circuit (EPROM). It is possible to change the configuration of the unit by altering the position of the switches and links within the unit.

Each *Diplomat jr* is supplied to meet the particular requirements of the purchaser as understood by Lucidata at the time of ordering. The details of this specific unit are given on page 4, together with a description of any special features.



Diplomat jr with top cover removed

Technical Data

Weight & Dimensions

Height x width x depth	25mm x 175mm x 110mm
Weight	390g

Electrical Requirements

Power to Diplomat jr	+5V DC at 500mA

Operating environment

Temperature	0-50°C
Humidity	0-90% non-condensing
For Indoor Use Only	

External connectors

Power	2.1mm socket
Port A	25-way D-type female connector (DTE) RS232 synch
Port B	25-way D-type female connector (DCE) RS232 asynch

External Indicators

Power on	LED indicating internal +5V present

Configuration

At power up	Internal switches and links set by the user

Data rates

Either Port	150 - 19200 bps in eight steps or external

Checking the Product

Before attempting to install your *Diplomat jr*, you should check the contents of the package. You should have:

Diplomat jr SA1TH unit
Power Adaptor
User Guide

If any of these are missing, contact Lucidata or your Lucidata appointed dealer.

Connecting to Port A

Port A can be found at one end of the unit, adjacent to the Power On LED. It is a 25-pin female D-type connector. It may be connected directly to a suitable synchronous device which must be configured as DCE.

Any connection restrictions and details of the pin assignments may be found in the *Technical Description* Section.

Connecting to Port B

Port B can be found at the other end of the unit, adjacent to the power-in connector. It is a 25 pin female D-type connector. It may be connected directly to a suitable asynchronous device which must be configured as DTE.

Any connection restrictions and details of the pin assignments may be found in the *Technical Description* Section.

Connecting the Power Supply

Connect the flying lead of the adaptor into the socket at the end of the unit. Plug the power adaptor into the mains supply after first verifying that voltages are compatible.

Switching On

When power is applied to the unit the red Power On LED should light. If it does not, check the supply . If the *Diplomat jr* is thought to be faulty, see *Service and Support* in the *Introduction.*

Configuration

Upon receipt, the *Diplomat jr* will already have been configured to your requirements. However, you may re-configure your unit, should your requirements change. Such a task is best undertaken by a person who is familiar with data communications products and terminology.

note ***If you re-configure your unit, you are advised to note the original switch settings in the Switch summary at the end of this section.***

Disconnect the *Diplomat jr* from the power supply!

Remove the four cross-head screws securing the cover to the base of the unit, using an appropriate screwdriver. Carefully remove the cover to expose the circuitry.

> **CAUTION!**
>
> **This unit contains devices which are static sensitive. Great care should be taken when adjusting switches and links to avoid touching any connections. Whenever possible, anti-static precautions should be taken, such as the use of an earthed wrist-strap and anti-static mat.**

You will observe that there are two white switch assemblies, with individual coloured sliders numbered 1 to 8. The convention used in this document to identify a particular switch and slider is of the form S1(4) which means switch S1 slider 4.

In addition to the switches there are a number of linking points which can be connected with jumpers. The position of all these is shown in the diagram on the summary pages at the end of this section.

All re-configuration takes place using these switches and links as described in this section. Both sets of switches are used, but a number of the links are only set during manufacture and should not be changed.

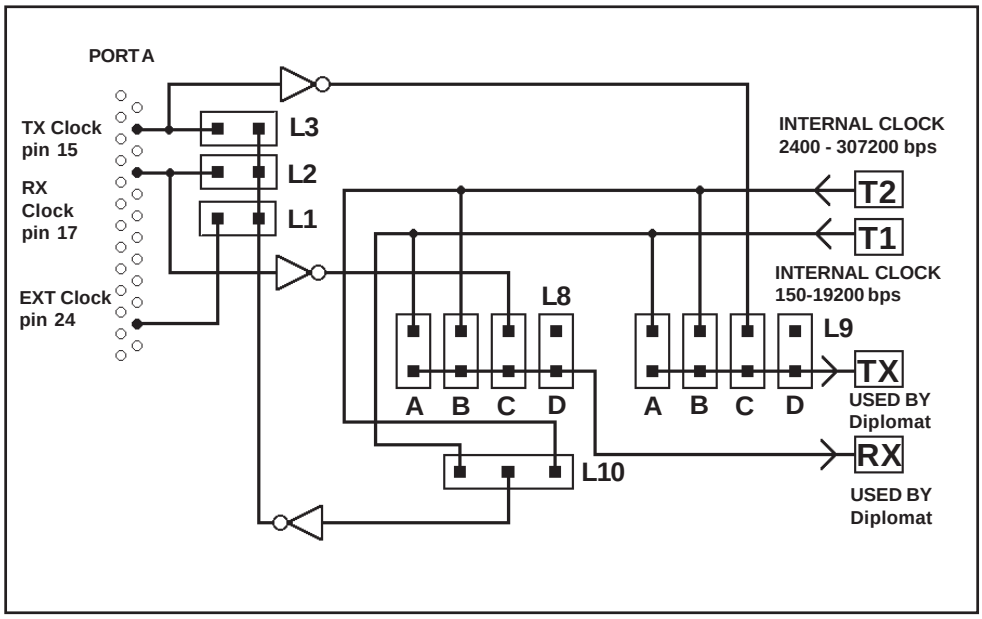
Clock Rates

Sliders 1,2, and 3 on Switches S1 and S2 are used to determine the frequencies of the two internal clocks T1 and T2 which can be used to determine data transmission speeds. T1 and T2 can each take eight values, dependent on the settings of the sliders.

Links L8, L9, L11 and L12 are used to determine which internal clocks (if any) are used. Links L1, L2, L3 and L10 determine which internal clocks (if any) are passed to the Port A and on which pin(s).

The Configuration Summary pages show the data rates obtainable with T1 and T2 for different settings of switches S1 and S2 sliders 1,2 and 3.

The following diagram illustrates the synchronous clock selection.



Character Format Port A

The character format of Port A is 8 bit characters bit synchronised with an external clock. Bit values are changed on the rising edge of the clock and sampled on the falling edge of the clock signal. Frame synchronisation is achieved from the idle state according to what mode has been set up on the configuration switch S1(7). If S1(7) is OFF then Character Synchronisation is selected. If S1(7) is ON then Bit Synchronisation is selected.

In Character Synchronisation mode an ASCII SYN character (16 hex) or EBCDIC SYN character (xx hex) synchronize the receiver to a byte boundary. In Bit Synchronisation mode an HDLC FLAG byte (7E hex) serves to synchronize the receiver to the byte boundary.

After synchronisation every 8 bits are then collected and presented as a new character. All leading SYN characters are discarded. Input on Port A is terminated according to how the unit is set up. In Character Synchronisation mode the input process recognises an ETX (03 hex) or DLE ETX (10 03 hex) dependant on the configuration settings. For the purpose of recognising these characters they are masked to 7 bits before testing to allow for different parities being used. The following two characters are also included in the data stream. The receiver is then reset so that it has to wait for another SYN character. The idle character transmitted is all ones.

In Bit Synchronisation mode termination may be by recognition of another HDLC FLAG (7E hex) or ABORT/IDLE line (FF hex).

In all modes external dropping of DCD is interpreted as end of transmission.

Switch S2(4) set OFF keeps RTS high and if it is set ON RTS only goes high when Port A is sending data.

Character Format Port B

Sliders 5 to 8 on switch S2 determine the character format for Port B.

slider	**5**	**ON**	**7 data bits**
		OFF	**8 data bits**
slider	**6**	**ON**	**No parity bits**
		OFF	**there is a parity bit**

slider	**7**	**8**	
	ON	**ON**	**0 parity bit (SPACE)**
	OFF	**ON**	**1 parity bit (MARK)**
	ON	**OFF**	**Even Parity**
	OFF	**OFF**	**Odd Parity**

Forwarding Control

Data flowing from Port B to Port A must be blocked in some way to prevent underflow and allow for continuous synchronisation. Several methods are possible and are determined using sliders 5 and 6 on switch S1.

slider	**5**	**6**	
	ON	**ON**	**RTS/DCD control HARDWARE (FDX)**
	ON	**OFF**	**Timeout control HARDWARE**
	OFF	**OFF**	**STX/ETX or IDLE FRAMING**
	OFF	**ON**	**DLE STX/DLE ETX or FLAG FRAMING**

The selections are described below.

RTS/DCD

While idling Port B keeps pin 8 (DCD) held low until it has characters to send. It then raises pin 8 and transmits the characters. Pin 8 is lowered a few milli-seconds after the last character is transmitted.

When Port B detects RTS going high it collects characters until RTS drops. The buffer contents are then transferred to Port A.

Timeout

Every time a character arrives on Port B a 50 milli-second dead-man-timer (DMT) is reset and the character is added to a buffer. When the DMT expires the buffer contents are transferred to Port A.

STX/ETX

The data characters are surrounded by the characters STX(02 hex) and ETX(03 hex) or DLE STX and DLE ETX both on transmission and reception on Port B. The values for these characters are masked to 7 bits in case of parity settings causing the 8th bit to be unpredictable, before they are tested.

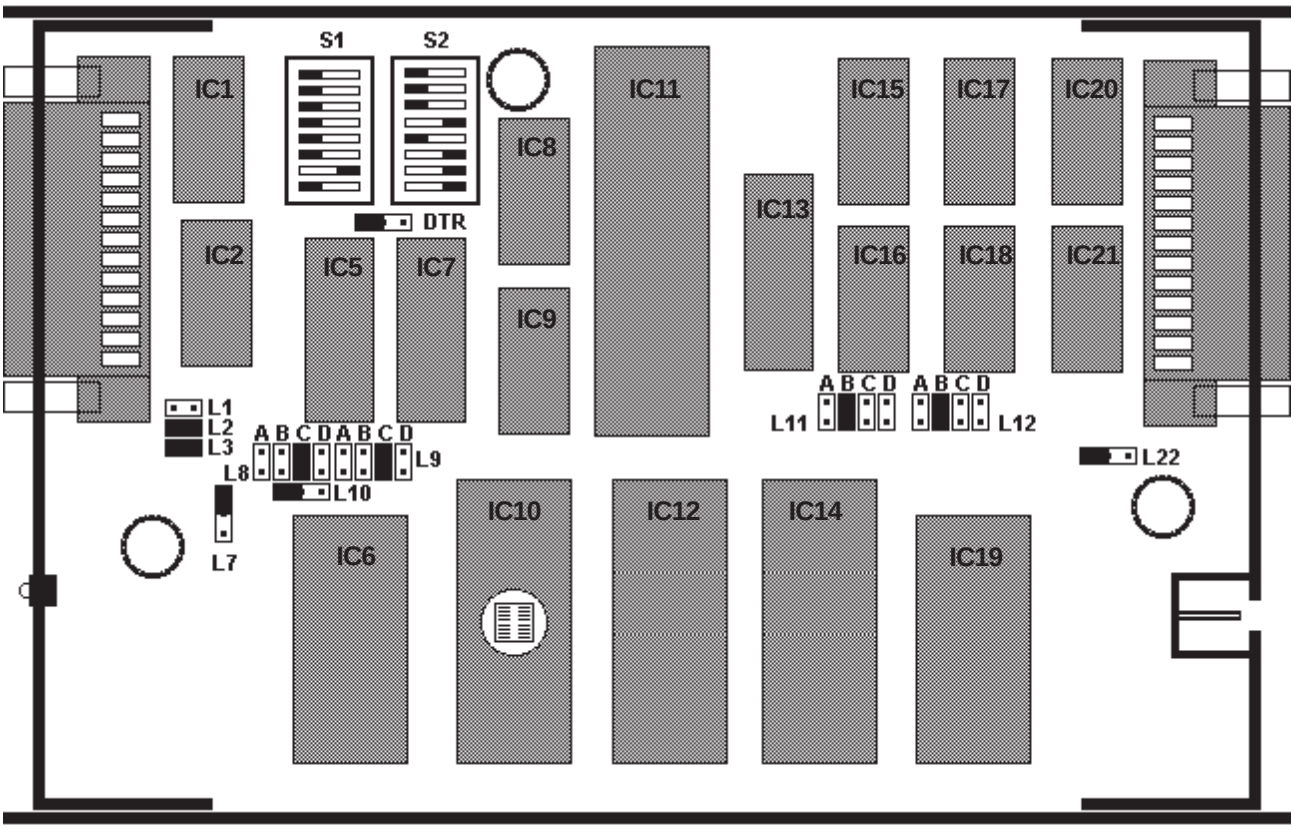
FLAG/IDLE

Data is accepted on Port B until either an HDLC FLAG (7E hex) or an ABORT code (FF hex) is received. The buffer contents are then transferred to Port A.

Refer to the Configuration Summary diagrams for the switch positions.

PORT A
HOST CONNECTOR

PORT B
TERMINAL CONNECTOR



JR SA1TH

Links L1, L2 and L3 - internal clock to host port

L1 pin-24 (internal clock output)
L2 pin-17 (receive clock)
L3 pin-15 (transmit clock)

Link L7 - RS232/RS422 Option

Link L7 is used to select the RS232 or RS422 receivers and transmitters for the synchronous port. If the upper two pins of L7 are linked the RS232 receiver is enabled. If the bottom two pins are linked, the RS422 receiver is enabled, if installed.

Link L8 - select source of RX Clock for host port

A connect to internal clock T1 (as set on switch S1)
B connect to internal clock T2 (as set on switch S2)
C connect to host port pin 17 (Receive Clock RX)
D not used on standard model

Link L9 - select source of TX Clock for host port

A connect to internal clock T1 (as set on switch S1)
B connect to internal clock T2 (as set on switch S2)
C connect to host port pin-15 (Transmit Clock TX)
D not used in the standard model.

Link L10 - Internal clock to outside world

If L10 is set so that the centre pin in connected to the pin nearest to the host port, internal clock T1 will be available to pass to the host port. If the centre pin is connected to the other pin, internal clock T2 will be available to pass to the host port.

Link L11 - select source of RX clock for terminal port

A connect to internal clock T1 (as set on switch S1)
B connect to internal clock T2 (as set on switch S2)
C connect to terminal port pin-17 (external receive clock)
D not used in the standard model

Link L12 - select source of TX clock for terminal port

A connect to internal clock T1 (as set on switch S1)
B connect to internal clock T2 (as set on switch S2)
C connect to terminal port pin-15 (external transmit clock)
D not used in the standard model

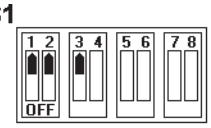
Link L22 - select source of the enabling signal for the terminal port

If L22 is left unstrapped, the transmitter is permanently enabled. If L22 is connected from the centre pin to the pin nearest to the host port, then pin20 of the terminal port exercises control on the transmitter. If L22 is connected from the centre pin to the pin nearest to the terminal port, then pin-19 of the terminal port exercises control on the transmitter.

DTR control option

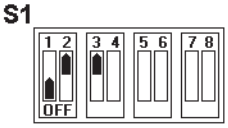
If the link on DTR is connecting the left two pins, then pin 20 on the host connector is held high as long as power is applied to the Diplomat jr. If the link is in the other position, then pin 20 on the host connector follows the state of either pin 19 or 20 on the terminal connector, depending on how Link 22 is set.

S1



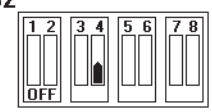
T1 150 sync

S1



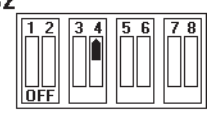
T1 300 sync

S2



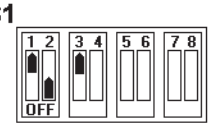
RTS High
PORT A

S2



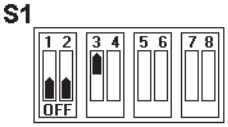
RTS Controlled
PORT A

S1



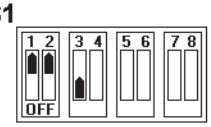
T1 600 sync

S1



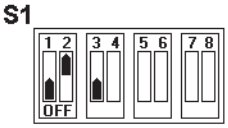
T1 1200 sync

S1



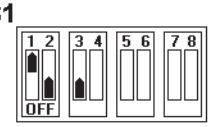
T1 2400 sync

S1



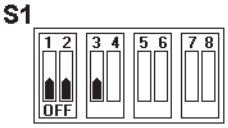
T1 4800 sync

S1



T1 9600 sync

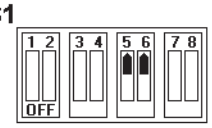
S1



T1 19200 sync

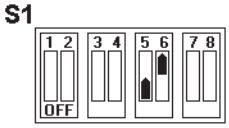
BIT SYNCHRONISED MODE

S1



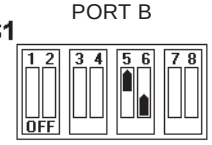
RTS/DCD Control
PORT B

S1



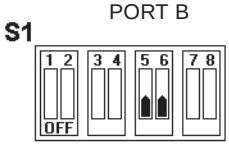
FLAG Framing
PORT B

S1



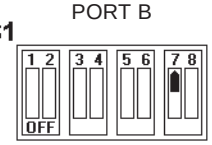
TIMEOUT Control
PORT B

S1



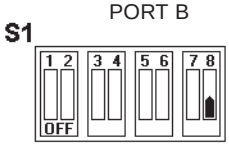
IDLE Framing
PORT B

S1



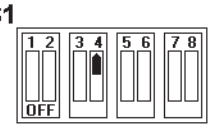
BIT SYNCH MODE

S1



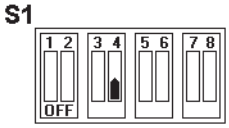
MUST BE OFF

S1



IDLE CHAR 7E
PORT A

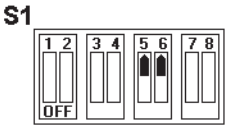
S1



IDLE CHAR FF
PORT A

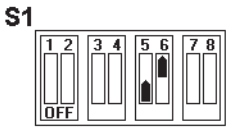
CHARACTER SYNCHRONISED MODE

S1



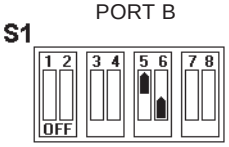
RTS/DCD Control
PORT B

S1



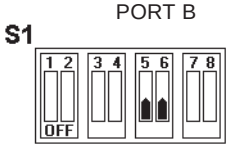
DLE STX/DLE ETX Framing
PORT B

S1



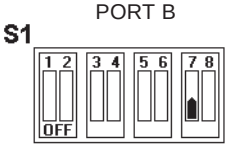
TIMEOUT Control
PORT B

S1



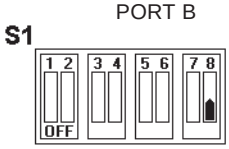
STX/ETX Framing
PORT B

S1



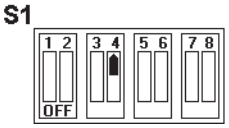
CHAR SYNCH MODE

S1



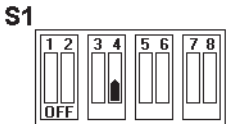
MUST BE OFF

S1

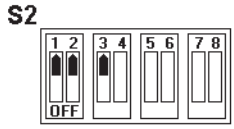


ASCII SYN
PORT A

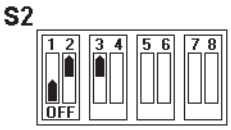
S1



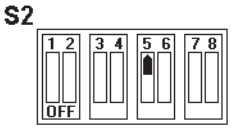
EBCDIC SYN
PORT A



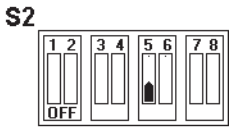
T2 150 async



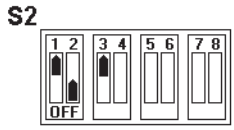
T2 300 async



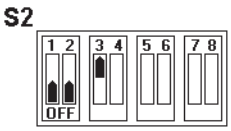
7 Data Bits
PORT B



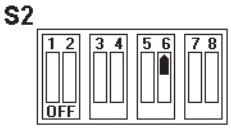
8 Data Bits
PORT B



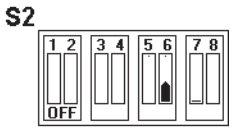
T2 600 async



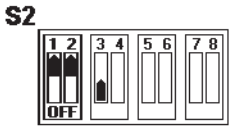
T2 1200 async



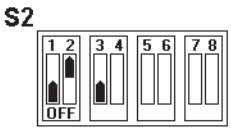
No Parity Bit
PORT B



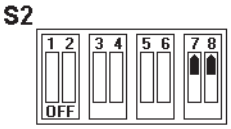
There is a Parity Bit
PORT B



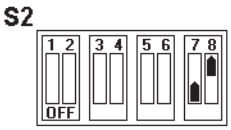
T2 2400 async



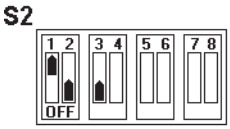
T2 4800 async



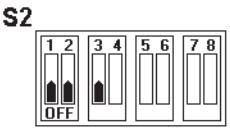
0 Parity Bit (SPACE)
PORT B



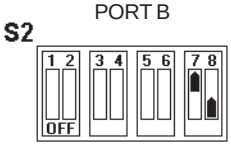
1 Parity Bit (MARK)
PORT B



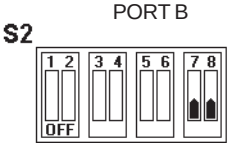
T2 9600 async



T2 19200 async



Even Parity
PORT B



Odd Parity
PORT B

Electrical Interfaces

Three connections are made to the *Diplomat jr* unit.

Port A

The table below shows the connections to the Port A connector.

This is a 25 pin Female D-Type connector configured as a serial synchronous DTE.

PIN NO.

1	*Protective Ground connects to chassis and power supply ground.*
2	*Synchronous Transmitted Data from the Diplomat*
3	*Synchronous Received Data going into the Diplomat*
4	*Request to Send is held high by the Diplomat when transmitting[3]*
5	*Clear to Send must be high to enable the Diplomat's transmitter[1]*
7	*Common signal return is connected to power supply ground*
8	*Data Carrier Detect must be high during sending to the Diplomat[2]*
15	*Transmit Clock required to strobe data out of the Diplomat*
17	*Receive Clock required to strobe data into the Diplomat*
20	*Data Terminal Ready held high by the Diplomat when powered up*
24	*Local clock output dependant on straps*

The minimum required signals for Port A are Pins 2(TXD), 3(RXD), 7(Common), 15(TXC) and 17(RXC). It is recommended that Protective Ground (pin 1) is also connected. Pins 5(CTS) and 8(DCD) are held high internally so that no connection need be made to them but if connection is made the following should be noted.

[1] The Diplomat cannot Transmit data on pin 2(TXD) if pin 5(CTS) is held low.

[2] The Diplomat will not see any data arriving on pin3 (RXD) if pin 8(DCD) is held low.

[3]Pin 4(RTS) is controlled by S2(4). If S2(4) is OFF, RTS is held high all the time. If S2(4) is ON, RTS only goes high while the Diplomat is transmitting data.

Clock signals must always be present on pins 15 and 17. The normal situation is that they are provided by the DCE equipment the Diplomat connects to so the links L2 and L3 should not be fitted. If the links L2 and L3 are fitted so that the Diplomat is the source of the clock signals on pins 15 and 17 then the DCE equipment must only have RS232 receivers connected to these lines. If both DCE and Diplomat provide clock signals then at best the system will not work and at worst damage to the circuitry on either side may result.

Note: This unit has links L2 and L3 installed so active clocks are present on pins 15 and 17.

Port B

The table below shows the connections to the Port B connector.

This is a 25 pin Female D-Type connector configured as a serial asynchronous DCE.

PIN NO.

1	*Protective Ground connects to chassis and power supply ground*
2	*Asynchronous Received Data going into the Diplomat*
3	*Asynchronous Transmitted Data from the Diplomat*
4	*Request To Send is held high if left open or controlled by terminal*[1]
5	*Clear to Send will be held high if pin 4 is high*
6	*Data Set Ready held high whilst power on*
7	*Common signal return is connected to power supply ground*
8	*Data Carrier Detect held high if Diplomat ready to send*[2]
15	**** Reserved *** Do NOT make any connection*
17	**** Reserved *** Do NOT make any connection*
19	If low[3] will disable Diplomat's transmitter
20	If low[3] will disable Diplomat's transmitter

The minimum required signals for Port B are Pins 2(TXD), 3(RXD) and 7(Common). It is recommended that Protective Ground (pin 1) is also connected. Pins 4(CTS), 8(DCD) and 20(DTR) are held high internally so that no connection need be made to them but if connection is made the following should be noted.

[1] Pins 4(RTS) and 5(CTS) are connected together and treated as RTS input. If RTS/DCD forwarding control is used ensure that pin 5(CTS) is left unconnected or is driven by the same signal as pin 4(RTS).

[2] Pin 8(DCD) is normally driven high all the time unless RTS/DCD forwarding control is being used.

[3] Pin 20(DTR) or pin 19 or neither of them being pulled low externally will disable the transmitter section of Port B. Which action occurs depends on the settings of L22 described earlier.

Power

2.1mm Coaxial Power Socket, positive centre pin.

Operation

On power-up the Diplomat performs some basic internal tests and then reads the switches S1 and S2. Note that this is only done at power-up so changing a setting while the power is on will have no effect and could cause accidental damage to the unit.

Provided that no signals exist to prevent operation of Port A, the Diplomat starts to transmit binary ones on pin 2 of Port A.
The units operates in full-duplex mode so data can appear at either interface at any time.

The Diplomat operates with two different types of synchronous data stream: Character Synchronised frames; Bit Synchronised frames. The type of data stream is determined by the setting of switch S1(7) which in turn alters the interpretation of the meaning of other sliders. If S1(7) is set to the OFF position Character Synchronisation is selected. If S1(7) is set to the ON position Bit Synchronisation is selected.

Character Synchronised Data Stream

The process controlling Port A waits for the appearance of a SYN character and then strips all SYN characters from the data stream until a non-SYN character is received. This character and all following characters are added to the Port B output buffer as they come in. When a termination sequence is detected two further characters are received and placed in the buffer. The input is then terminated by resetting the receiver of Port A. It is necessary for the receiver to be re-synchronised, with a SYN, before it can receive more data. If the bit rates are the same on Port A and Port B and the data flow from Port A is continuous then the Port B output buffer will gradually fill as it has to shift 10 bits (8N1) out for every 8 bits received by Port A. However the buffer will hold approximately 15000 characters so even quite long bursts of continuous activity will be accommodated. The other alternative is to ensure that the Port B bit rate is higher than the Port A bit rate.

The process controlling Port B can handle different methods to delimit a data packet according to the configuration settings but the intended method is as follows: As characters are received on Port B they are added to the Port A output buffer but not released to it. When a termination condition has been reached, such as receiving the characters DLE ETX and two other characters, the buffer is released to the Port A output process. This inserts four SYN characters before outputing the collected data to the line. If more data comes in on Port B immediately it is collected in the normal way but will only be released to the Port A output process if it is idle. If the Port B input data are effectively only response data to Port A input then there should never be a problem. The ultimate timing of these processes must reside with the external applications as no algorithm has been provided.

This process will continue until the unit is powered down.

Bit Synchronised Data Stream

The process controlling Port A waits for the appearance of the HDLC Flag sequence 01111110 (7E hex) which serves to synchronise the receiver on a byte boundary. This byte and all following bytes are added to the Port B output buffer as they come in and will be transmitted immediately if the Port B interface is enabled. When the selected termination condition is detected, another HDLC FLAG sequence or an ABORT/IDLE sequence 11111111 (FF hex), the Port A receiver is reset so that it has to wait for the start of another frame starting with an HDLC Flag. It is important that the sending device leaves a gap between frames otherwise the new synchronising flag may not be seen and a block will be lost.

If the bit rates are the same on Port A and Port B and the data flow from Port A is continuous then the Port B output buffer will gradually fill as it has to shift 10 bits (8N1) out for every 8 bits received by Port A. However the buffer will hold approximately 15000 characters so even quite long bursts of continuous activity will be accommodated. The other alternative is to ensure that the Port B bit rate is higher than the Port A bit rate.

The process controlling Port B can handle different methods to delimit a data packet as selected by the configuration switches. As characters are received on Port B they are added to the Port A output buffer but not released to it. When one of the termination conditions has been reached, such as receiving the HDLC FLAG or ABORT character, the buffer is released to the Port A output process. This process sends the collected data block as a single transmission. If more data immediately comes in on Port B it is collected in the normal way but will only be released to the Port A output process when properly terminated.

This process will continue until the unit is powered down.

Diplomat jr model SA1TH specification

Revision 1.0
Date 21/08/06

1.0 Introduction

This document describes the operation of a Lucidata Diplomat jr when running the SA1TH firmware revision 1.00. This firmware is based on the model SA1ID revision 1.01 firmware and includes additional support for HDLC. The purpose of the device is to take an HDLC block of serial synchronous data arriving at the synchronous RS232 port (Port A), and send it out over the serial asynchronous RS232 port (Port B). It is also required to accept blocks of asynchronous 8 bit characters from Port B and package them up for transmission from Port A. Configuration of the Diplomat jr is achieved using the two sets of DIP switches (16 switches) inside the Diplomat jr.

2.0 Configuration

Asynchronous transmission speeds may be selected by setting up internal switches to choose from the set: 150,300,600,1200,2400,4800,9600,19200 bps. Other values may be requested after discussion.

Asynchronous character format can be selected from the following set: 8N1, 8N2, 8E1, 8O1.

Synchronous data rates are determined by the clock speed provided by the external equipment onto pins 15 and 17 of Port A. If jumpers are set inside the Diplomat the internal clock can be used to drive pins 15 and 17 thus supplying a clock for the external equipment.

The framing of the asynchronous block can be selected to be by hardware, by inband data or timeout according to switch settings.

2.1 Asynchronous Blocking

If hardware control is selected the Diplomat will keep pin 8 (DCD) on Port B low (spacing) until it has something to send. It will then raise pin 8, send any buffered characters and lower pin 8. Reception is indicated by the Diplomat sensing pin 4 (RTS) rising. The Diplomat will collect all the characters that arrive until pin 4 drops again. It will then pass on the compete block to Port A.

If Framing is selected the Diplomat will collect characters from Port B until it finds the FLAG (7E hex) or the ABORT (FF hex) character. It will then pass on the collected characters to Port A.

If No Framing is used characters are collected from Port B until there is a delay of more than 50 milliseconds. All collected characters are then passed on to Port A. It is the responsibility of the asynchronous source to provide correctly formatted HDLC frames as no HDLC specific hardware is present in the Diplomat.

3.0 Synchronous Operation

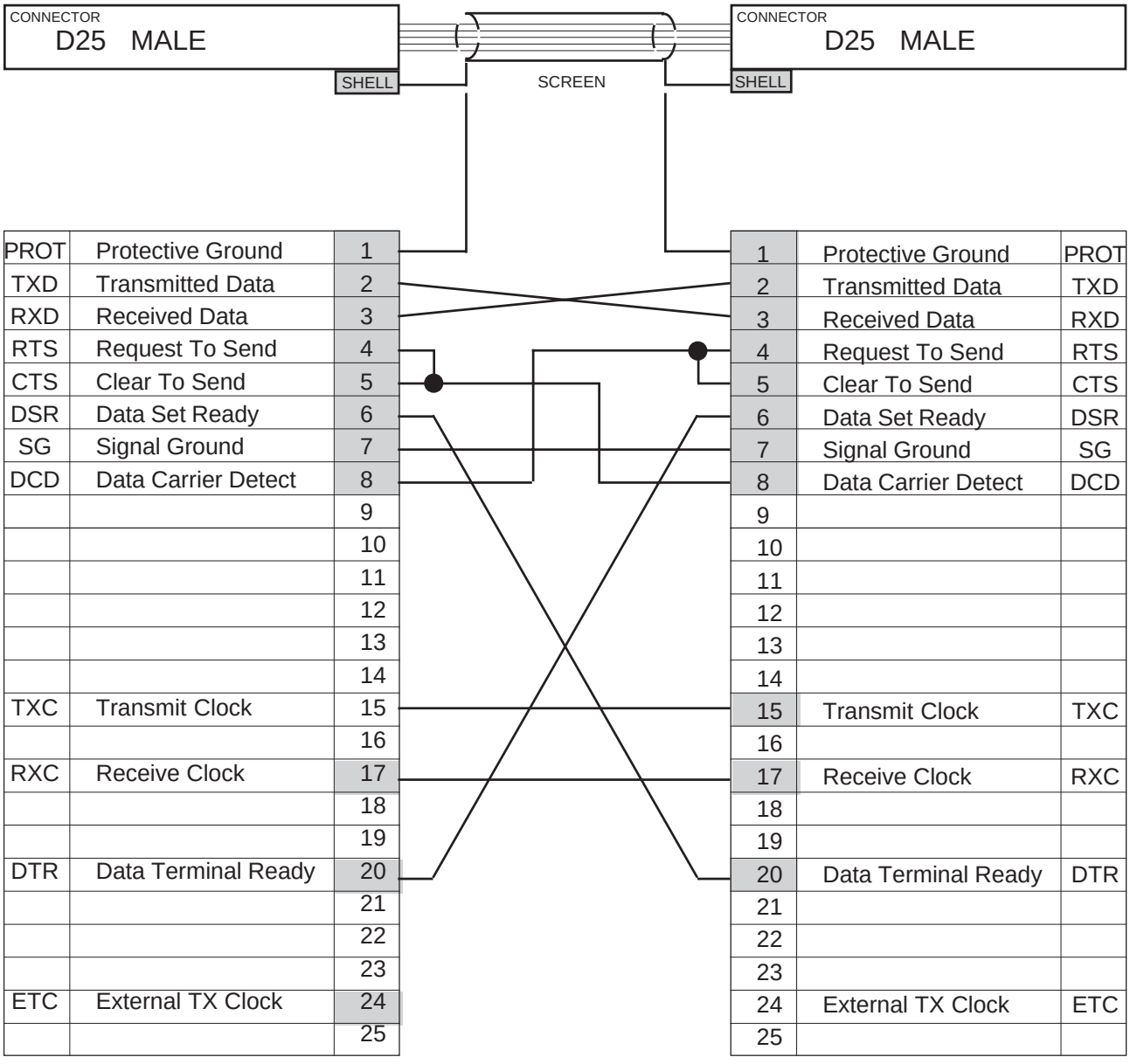
At power up the Diplomat will start sending an idle pattern of all ones out on Port A. When it has received a correctly formed block of characters from Port B it will send out the block to Port A. Bits are transmitted Least Significant Bit first and the data state of the RS232 TX line is changed on the rising edge of the TX clock.

The Diplomat listens to the synchronous line until it sees an HDLC FLAG character (7E hex) and then starts to extract and pack 8 bits at a time into the output buffer of Port B. When the selected termination condition is detected or DCD drops the receiver is reset to force resynchronisation. The RS232 RX line is sampled on the falling edge of the RX clock. All the characters are forwarded to Port B. The reverse process is applied when sending data from Port B to Port A.

DESCRIPTION
DIRECT CONNECT SYNCHRONOUS RS232

FROM
Diplomat jr (DTE) PORT A

TO
SYNCHRONOUS (DTE)



PROT	Protective Ground	1	1	Protective Ground	PROT
TXD	Transmitted Data	2	2	Transmitted Data	TXD
RXD	Received Data	3	3	Received Data	RXD
RTS	Request To Send	4	4	Request To Send	RTS
CTS	Clear To Send	5	5	Clear To Send	CTS
DSR	Data Set Ready	6	6	Data Set Ready	DSR
SG	Signal Ground	7	7	Signal Ground	SG
DCD	Data Carrier Detect	8	8	Data Carrier Detect	DCD
		9	9		
		10	10		
		11	11		
		12	12		
		13	13		
		14	14		
TXC	Transmit Clock	15	15	Transmit Clock	TXC
		16	16		
RXC	Receive Clock	17	17	Receive Clock	RXC
		18	18		
		19	19		
DTR	Data Terminal Ready	20	20	Data Terminal Ready	DTR
		21	21		
		22	22		
		23	23		
ETC	External TX Clock	24	24	External TX Clock	ETC
		25	25		

Note: It cannot be assumed that unlabelled pins can be used and no connections should be made to them.

DESCRIPTION

DIRECT CONNECT ASYNCHRONOUS RS232

FROM
PC COM PORT (DTE)

TO
Diplomat jr (DCE) PORT B

DCD	Data Carrier Detect	1
RXD	Received Data	2
TXD	Transmitted Data	3
DTR	Data Terminal Ready	4
SG	Signal Ground	5
DSR	Data Set Ready	6
RTS	Request To Send	7
CTS	Clear To Send	8
RI	Ring Indicator	9

1	Protective Ground	PROT
2	Transmitted Data	TXD
3	Received Data	RXD
4	Request To Send	RTS
5	Clear To Send	CTS
6	Data Set Ready	DSR
7	Signal Ground	SG
8	Data Carrier Detect	DCD
9		
10		
11		
12		
13		
14		
15	Transmit Clock	TXC
16		
17	Receive Clock	RXC
18		
19		
20	Data Terminal Ready	DTR
21		
22		
23		
24	External TX Clock	ETC
25		

Note: It cannot be assumed that unlabelled pins can be used and no connections should be made to them.